CLAIMS

What is claimed is:

1. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a contact etch stop over said layer of metal;

reacting said layer of metal with said contact etch stop; and

removing unreacted metal from said layer of metal to form said local interconnect.

2. The process of claim 1, wherein said contact etch stop comprises a metal silicide.

3. The process of claim 1, further comprising the step of patterning said contact etch stop to form the boundaries of said local interconnect.

4. The process of claim 3, wherein said step of patterning said contact etch stop to form the boundaries of said local interconnect is performed prior to said step of reacting said layer of metal with said contact etch stop.

5. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a layer of metal silicide over said layer of metal;

reacting said layer of metal silicide with said layer of metal; and

removing unreacted metal remaining from said layer of metal to form said local interconnect.

6. The process of claim 5, wherein said layer of metal comprises a refractory metal.

7. The process of claim 6, wherein said refractory metal is selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium.

8. The process of claim 7, wherein said refractory metal comprises titanium.

9. The process of claim 5, wherein said layer of metal has a thickness in the range of about 200 Angstroms to about 600 Angstroms.

10. The process of claim 9, wherein said layer of metal has a thickness of approximately 300 Angstroms.

11. The process of claim 5, wherein said layer of metal silicide comprises tungsten silicide.

12. The process of claim 5, wherein said layer of metal silicide has a thickness in the range of about 500 Angstroms to about 1200 Angstroms.

13. The process of claim 12, wherein said layer of metal silicide has a thickness in the range of about 600 Angstroms to about 700 Angstroms.

14. The process of claim 5, wherein said step of reacting said layer of metal silicide with said layer of metal comprises annealing said layer of metal silicide and said layer of metal at a temperature ranging from about 600°C to about 700°C.

15. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer by chemical vapor deposition (CVD);

forming a layer of metal silicide over said layer of metal by CVD;

patterning said layer of metal silicide;

reacting said metal silicide with said layer of metal; and

removing unreacted metal remaining from said layer of metal to form said local interconnect.

16. The process of claim 15, wherein said step of forming a layer of metal over said at least one semiconductor layer by CVD and said step of forming a layer of metal silicide over said layer of metal by CVD are carried out in the same vacuum environment.

17. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of metal;

annealing said layer of first metal silicide and said layer of metal to form a composite structure; and

removing remaining metal from said layer of metal to form said local interconnect.

18. The process of claim 17, wherein said composite structure comprises said first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said layer of metal and metal from said first metal silicide.

19. The process of claim 18, wherein said layer of metal comprises titanium and said first metal silicide comprises tungsten silicide, such that said composite structure comprises tungsten silicide, titanium silicide, and titanium tungsten intermetallic compound.

20. The process of claim 17, further comprising the step of patterning said layer of first metal silicide to form a boundary of said local interconnect.

21. The process of claim 20, wherein said step of patterning said layer of first metal silicide to form a boundary of said local interconnect is performed prior to said step of annealing said layer of first metal silicide and said layer of metal to form a composite structure

22. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of said local interconnect;

annealing said patterned first metal silicide and said layer of refractory metal to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said local interconnect.

23. The process of claim 22, wherein said step of patterning said layer of first metal silicide to define a boundary of said local interconnect comprises the step of selectively etching said layer of first metal silicide.

24. The process of claim 23, wherein said step of selectively etching said layer of first metal silicide comprises the step of dry etching said layer of first metal silicide.

25. The process of claim 22, wherein said step of annealing said patterned first metal silicide and said layer of refractory metal to form a composite structure is carried out in an atmosphere of reactive nitrogen such that at least remaining refractory metal from said layer of refractory metal is nitrified.

26. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of titanium over said at least one semiconductor layer, said layer of titanium having a thickness ranging from about 200 Angstroms to about 600 Angstroms;

forming a mask layer of tungsten silicide over said layer of titanium, said mask layer of tungsten silicide having a thickness ranging from about 500 Angstroms to about 1200 Angstroms;

selectively etching said mask layer to define a boundary of said local interconnect;

annealing said mask layer and said layer of titanium in an atmosphere of reactive nitrogen thereby forming a composite structure where said mask layer contacts said layer of titanium and nitrifying at least said layer of titanium not covered by said mask layer to form a layer of titanium nitride, said composite structure comprising titanium silicide, tungsten silicide and a titanium tungsten intermetallic compound; and

removing said layer of titanium nitride and underlying titanium to form said local interconnect.

27. A process of forming a semiconductor device comprising:

providing a substrate assembly having at least one semiconductor layer;

forming source and drain regions of a field effect transistor in said at least one semiconductor layer;

forming a gate oxide over said at least one semiconductor layer;

forming a gate contact over said gate oxide;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of metal;

patterning said layer of first metal silicide to define a boundary of a local interconnect;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said local interconnect.

28. The process of claim 27, wherein said local interconnect connects at least one of said source, drain, and gate to another active area within said substrate assembly.

29. A process of forming a memory array, said memory array comprising a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor, said process comprising:

providing at least one semiconductor layer;

forming sources, drains and gates for each of said field effect transistors over said at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of at least one local interconnect;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining metal from said layer of refractory metal to form said at least one local interconnect, said at least one local interconnect connecting at least one of said source, drain and gate of one of said field effect transistors with another active area of said memory array.

30. A process of fabricating a wafer comprising:

providing a wafer having a substrate assembly, said substrate assembly having at least one semiconductor layer;

forming a repeating series of sources, drains and gates for at least one field effect transistor on each of a plurality of individual die on said wafer over said at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of at least one local interconnect in each of said individual die;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said at least one local interconnect in each of said individual die, said at least one local interconnect in each of said individual die connecting at least one of said source, drain and gate of one of said field effect transistors with another active area in each of said individual die.

31. A local interconnect comprising:

a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said first metal silicide and metal from said second metal silicide.

32. The local interconnect of claim 31, wherein said first metal silicide and said second metal silicide each comprise at least one refractory metal.

33. The local interconnect of claim 32, wherein said at least one refractory metal for said first metal silicide and said second metal silicide is selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium.

34. The local interconnect of claim 32, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

35. A local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly, said first and second active semiconductor regions being separated by an insulating region, said local interconnect comprising:

a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, said refractory metal from said first refractory metal silicide being different from said refractory metal from said second refractor metal silicide.

36. The local interconnect of claim 35, wherein said composite structure has a thickness in the range of about 700 Angstroms to about 1800 Angstroms.

37. A semiconductor device comprising:

a substrate assembly having at least one semiconductor layer;

at least one field effect transistor formed in said at least one semiconductor layer, said least one field effect transistor having a source, a drain and a gate; and

a local interconnect for connecting at least one of said source, said drain and said gate to another active area within said substrate assembly, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide.

38. A memory array comprising:

a plurality of memory cells arranged in rows and columns and formed on a substrate assembly having at least one semiconductor layer, each of said plurality of memory cells comprising at least one field effect transistor; and

at least one local interconnect for connecting at least one of a source, a drain and a gate of said at least one field effect transistor in one of said plurality of memory cells to one of an active area within said one memory cell or to one of a source, a drain and a gate of said at least one field effect transistor in another one of said plurality of memory cells, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide.

39. The memory array of claim 38, further comprising a plurality of local interconnects for connecting additional active areas within each of said plurality of memory cells.

40. The memory array of claim 38, further comprising a plurality of local interconnects for connecting together active areas from different memory cells.